REMARKS

Claims 1-12 and 16-30 are pending. The Examiner's reconsideration of the rejections is respectfully requested in view of the amendments and remarks.

Claims 1-12 and 16-27 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner stated essentially that "transformation" used in claims 1 and 16 in the claims in an incomplete structure.

Claims 1 and 16 claim, *inter alia*, "specifying a transformation behavior applied to the design objects; processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design; and outputting a transformed hierarchical very large scale integrated design."

Claims 1 and 16 have been clarified to point out that the transformation behavior is preformed on the hierarchical very large scale integrated design and that a transformed hierarchical very large scale integrated design is output. Any transformation behavior may be applied on the hierarchical very large scale integrated design, however, such a transformation behavior is to be applied in a top-down processing. An example of a transformation behavior resolves boundary conditions between design elements in the hierarchical very large scale integrated design; any number of additional transformation behaviors are possible. No know system or method processes, top-down, a graph to perform a transformation behavior on a hierarchical very large scale integrated design. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 1, 2, 16 and 17 have been rejected under 35 U.S.C. 102(e) as being anticipated by Bartels et al. (U.S. Patent No. 6,263,480). The Examiner stated essentially that Bartels teaches all the limitations of claims 1, 2, 16 and 17.

Claims 1 and 16 claim, *inter alia*, "specifying a transformation behavior applied to the design objects; processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design; and outputting a transformed hierarchical very large scale integrated design."

Bartels teaches a method for tracing shorts in a VLSI design (see Abstract). Bartels does not teach "processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design" as claimed in claims 1 and 16. Bartels outputs a traced short in the VLSI design (see col. 3, lines 15-21). Bartels graphing techniques build a list of objects describing a path or short (see Figure 4); such a path is a portion of the hierarchical net. The path through the hierarchical net and is not a transformed hierarchical net. The list of objects has no effect on a design of the hierarchical net. Therefore, Bartels fails to teach "processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design" as claimed in claims 1 and 16.

Claim 2 depends from claim 1. Claim 17 depends from claim 16. The dependent claims are believed to be allowable for at least the reasons given for claims 1 and 16. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 1-12 and 16-27 have been rejected under 35 U.S.C. 102(b) as being anticipated by Russell et al. (U.S. Patent No. 5,519,628). The Examiner stated essentially that Russell teaches all the limitations of claims 1-12 and 16-27.

Claims 1 and 16 claim, *inter alia*, "specifying a transformation behavior applied to the

design objects; processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design; and outputting a transformed hierarchical very large scale integrated design."

Russell teaches methods for VLSI circuit design checking (see col. 6, liens 26-37). Russell does not teach "processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design" as claimed in claims 1 and 16. Russell teaches a top-down analysis for a tree layout (see col. 22, lines 14-28). An analysis of a tree layout is not analogous to performing a transformation behavior on a hierarchical very large scale integrated device, essentially as claimed in claims 1 and 16. A mere analysis does not perform a transformation behavior. Therefore, Russell fails to teach all the limitations of claims 1 and 16.

Claims 2-11 depend from claim 1. Claims 17-27 depend from claim 16. The dependent claims are believed to be allowable for at least the reasons given for claims 1 and 16. At least claims 8 and 23 are believed to be allowable for additional reasons.

Claims 8 and 23 claim "wherein processing, top-down, the graph comprises resolving boundary conditions, recursively, by adjusting a parent cell, beginning with a root cell of the graph."

Russell teaches methods for VLSI circuit design checking (see col. 6, liens 26-37). Russell does not teach "resolving boundary conditions, recursively, by adjusting a parent cell, beginning with a root cell of the graph" as claimed in claims 8 and 23. Russell's analysis processes whatever ground rule it has been given to check for compliance; including manipulation of fragmented shape data to understand complex shapes (see col. 11, lines 30-41). The manipulation of data is not analogous to adjusting a parent cell; the manipulation of data changes the data's form (e.g., from small segments within a VLSI to a nested framework) but not the underlying

information. Russell does not teach adjusting a design. Therefore, Russell fails to teach "resolving boundary conditions, recursively, by adjusting a parent cell, beginning with a root cell of the graph" as claimed in claims 8 and 23.

Reconsideration of the rejection is respectfully requested.

Claims 1, 3-12, 16 and 18-27 have been rejected under 35 U.S.C. 102(e) as being anticipated by Teig et al. (U.S. Patent Application No. 2004/0123260). The Examiner stated essentially that Teig teaches all the limitations of claims 1, 3-12, 16 and 18-27.

Claims 1 and 16 claim, *inter alia*, "specifying a transformation behavior applied to the design objects; processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design; and outputting a transformed hierarchical very large scale integrated design."

Teig teaches a method for considering diagonal wiring in calculating a placement-configuration costs (see paragraph [0036] and [0095]). Teig does not teach "processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design" as claimed in claims 1 and 16. Similar to Russell above, Teig teaches a method for analyzing a layout. Similar to Russell, Teig's analysis does not teach a method for transforming a VSLI, much less processing, top-down, the graph to perform the transformation behavior on the hierarchical very large scale integrated design, essentially as claimed in claims 1 and 16. Therefore, Teig fails to teach all the limitations of claims 1 and 16.

Claims 3-12 depend from claim 1. Claims 18-27 depend from claim 16. The dependent claims are believed to be allowable for at least the reasons given for claims 1 and 16. At least claims 8 and 23 are believed to be allowable for additional reasons.

Claims 8 and 23 claim "wherein processing, top-down, the graph comprises resolving boundary conditions, recursively, by adjusting a parent cell, beginning with a root cell of the graph."

Teig teaches a method for considering diagonal wiring in calculating a placement-configuration costs (see paragraph [0036] and [0095]). Teig does not teach "resolving boundary conditions, recursively, by adjusting a parent cell, beginning with a root cell of the graph" as claimed in claims 8 and 123. Teig teaches a method for analyzing a layout. Nowhere does Teig teach adjusting a cell of a layout. Teig does not teach a method including adjusting a parent cell, essentially as claimed in claims 8 and 23. Therefore, Teig fails to teach all the limitations of claims 8 and 23.

Reconsideration of the rejection is respectfully requested.

New claims 28-30 are believed to be in condition for allowance.

Claim 28 claims, *inter alia*, "processing the graph top-down beginning with a root cell of the graph to perform the transformation behavior on the hierarchical very large scale integrated design, wherein the transformation behavior resolves a boundary condition of the hierarchical very large scale integrated design by performing a move operation, a split operation or a merge operation to adjust the structure of the hierarchical very large scale integrated design."

The teachings of Bartels, Russell and Teig, either individually or in combination fail to teach that a transformation behavior resolves a boundary condition of the hierarchical very large scale integrated design by performing a move operation, a split operation or a merge operation to adjust the structure of the hierarchical very large scale integrated design, as claimed in claim 28. The teachings of Bartels, Russell and Teig teach analysis of VSLI designs. These teachings fail

Claims 29 and 30 depend from claim 28. The dependent claims are believed to be allowable for at least the reasons given from claim 28.

For the forgoing reasons, the present application, including claims 1-12 and 16-30, is believed to be in condition for allowance. The Examiner's early and favorable action is respectfully urged.

Respectfully submitted,

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